Atty. Docket No. MP0351
Application No: 10/776,476

Amendments to the Claims

Please amend the claims as follows:

1. (Previously Presented) An adjustable, segmented amplifier, comprising:
   a) a first fixed stage configured to amplify an analog signal and provide a first amplified output at a first common node; and
   b) an adjustable stage comprising a plurality of independently selectable parallel amplifier segments, each of said parallel amplifier segments having an input at said first common node and an output at a second common node, wherein each of said parallel amplifier segments comprises (i) a transistor having a control terminal, and (ii) a first inductor configured to resonate with a capacitance at a base of said transistor and in electrical communication with said control terminal of said transistor, and said adjustable stage is configured to provide an output signal in one of a plurality of power ranges corresponding to a number of selected parallel amplifier segments, said output signal having a minimum power efficiency when two or more of said parallel amplifier segments are selected.

2. (Previously Presented) The system of Claim 41, wherein each of said parallel amplifier segments comprises a transistor having a control terminal, and said adjustable stage comprises a first inductor in electrical communication with said control terminal of at least one of said transistors.

3. (Previously Presented) The adjustable amplifier of Claim 9, wherein each of said parallel amplifier segments further comprises a capacitor in electrical communication with said first common node and said control terminal of said transistor.

4. (Previously Presented) The adjustable amplifier of Claim 9, wherein the remainder of each of said parallel amplifier segments comprises second inductor in electrical communication with said control terminal of said transistor.

5. (Previously Presented) The adjustable amplifier of Claim 4, wherein each of said parallel amplifier stages further comprises a bias circuit in electrical communication with said first and second inductors.

6. (Original) The adjustable amplifier of Claim 1, wherein at least one of said plurality of parallel amplifier segments is selected for operation.

7. (Original) The adjustable amplifier of Claim 6, wherein said at least one selected parallel amplifier segment is selected for operation by applying a non-zero bias at a control terminal thereof.

8. (Original) The adjustable amplifier of Claim 7, further comprising a bias generator configured to apply a bias to said control terminal.

9. (Currently Amended) An adjustable, segmented amplifier, comprising:
   a) a first fixed stage configured to amplify an analog signal and provide a first amplified output at a first common node;
   b) an adjustable stage comprising a first inductor and a plurality of independently selectable parallel amplifier segments, each of said parallel amplifier segments having an input at said first common node, an output at a second common node and a transistor having a control terminal, wherein said first inductor is in electrical communication with said control terminal of at least one of said transistors and said adjustable stage is configured to provide an output signal in one of a plurality of power ranges corresponding to a number of selected parallel amplifier segments, said output signal having a minimum power efficiency when

two or more of said parallel amplifier segments are selected, wherein at least one selected parallel amplifier segment is selected for operation by applying a non-zero bias at the control terminal thereof; and

c) a bias generator comprising a current source ~~mirror~~ configured to apply said bias to said control terminal.

10. (Currently Amended) The adjustable amplifier of Claim 9, wherein said bias generator further comprises a buffer transistor configured to receive an output from said current source ~~mirror~~ and provide said bias.

11. (Currently Amended) The adjustable amplifier of Claim 9, ~~further comprising a~~ wherein said current source comprises a current mirror.

12. (Currently Amended) The adjustable amplifier of Claim 11, wherein said current source further comprises a programmable digital-to-analog converter.

13. (Original) The adjustable amplifier of Claim 1, wherein an efficiency of said high-efficiency output power range is at least 50% of a maximum efficiency of said adjustable amplifier.

14. (Original) The adjustable amplifier of Claim 13, wherein said efficiency is at least 60% of said maximum efficiency.

15. (Original) The adjustable amplifier of Claim 1, wherein said fixed stage comprises a first bipolar transistor and each of said plurality of parallel amplifier segments comprises a second bipolar transistor.

16. (Previously Presented) The adjustable amplifier of Claim 15, further comprising:

a) a second inductor in electrical communication between said first bipolar transistor and a first electric potential; and wherein

b) the first inductor is in electrical communication between each of said second bipolar transistors and said first electric potential.

17. (Previously Presented) The adjustable amplifier of Claim 1, wherein each of said plurality of parallel amplifier segments has one or more substantially identical characteristics as the others of said plurality of parallel amplifier segments.

18. (Previously Presented) A circuit, comprising:

a) means for amplifying an analog signal to provide a first amplified signal;

b) means for providing an adjustably amplified output from said first amplified signal; and

c) means for selecting an output power range for said adjustably amplified output comprising a plurality of parallel, independently selectable means for further amplifying said first amplified signal, each of said parallel means for further amplifying comprising (i) an input at a first common node, (ii) a transistor having a control terminal, (iii) an inductor configured to resonate with a capacitance at a base of said transistor, coupled to said control terminal of said transistor to a bias signal, and (iv) an output at a second common node.

19. (Previously Presented) The circuit of Claim 18, each of said parallel means for further amplifying having an input at a first common node and an output at a second common node.

20. (Previously Presented) The circuit of Claim 26, wherein said adjustably amplified output has one of a plurality of power ranges corresponding to a number of selected means for further amplifying, said output signal having a minimum power efficiency when two or more of said means for further amplifying are selected.

21. (Original) The circuit of Claim 20, having a power efficiency of at least 50% of a maximum efficiency of said circuit.

22. (Original) The circuit of Claim 19, wherein each of said means for further amplifying comprises a transistor having a control terminal, and said circuit further comprises a first means for coupling said control terminal of at least one of said transistors to a first bias.

23. (Previously Presented) The circuit of Claim 18, wherein each of said means for further amplifying further comprises a means for filtering said first amplified signal in electrical communication with said first common node and said control terminal of said transistor.

24. (Previously Presented) The circuit of Claim 18, wherein each of said means for further amplifying comprises a first means for coupling said control terminal of said transistor to a bias signal.

25. (Previously Presented) The circuit of Claim 18, further comprising a means for providing said bias signal.

26. (Currently Amended) A circuit, comprising:

a) means for amplifying an analog signal to provide a first amplified signal;

b) means for providing an adjustably amplified output from said first amplified signal, comprising a plurality of parallel, independently selectable means for further amplifying said first amplified signal and a first means for coupling at least one of said parallel means for further amplifying to a first bias, each of said parallel means for further amplifying comprising a transistor having a control terminal, having an input at a first common node and an output at a second common node;

c) a first inductor in electrical communication with said control terminal of at least one of said transistors;

d) means for selecting an output power range for said adjustably amplified output, said adjustably amplified output having a minimum power efficiency when two or more of said means for further amplifying are selected; and

e) means for providing a bias signal comprising a current source ~~mirror~~ and a means for providing a current to said current source~~mirror~~.

27. (Currently Amended) The circuit of Claim 26, wherein said means for providing said bias signal further comprises a means for buffering an output from said current source~~mirror~~.

28. (Previously Presented) The circuit of Claim 26, wherein at least one of said plurality of means for further amplifying is selected for operation.

29. (Previously Presented) The circuit of Claim 18, wherein said means for amplifying comprises a first bipolar transistor and each of said means for further amplifying comprises a second bipolar transistor.

30. (Original) The circuit of Claim 29, further comprising:

a) a first means for coupling an output matching network to an output of said means for amplifying; and

b) a corresponding second means for coupling a control gate of each of said second bipolar transistors to a bias signal.

31. (Previously Presented) The circuit of Claim 18, wherein each of said means for further amplifying has one or more substantially identical characteristics as the other(s) of said means for further amplifying.

32. (Original) An integrated circuit, comprising:
    a) the adjustable amplifier of Claim 1; and
    b) a transmitter communicatively coupled to said adjustable amplifier, said transmitter being configured to transmit said analog signal to said adjustable amplifier.

33. (Original) The integrated circuit of Claim 32, wherein said analog signal has a frequency of at least about 800 MHz.

34. (Original) The integrated circuit of Claim 32, wherein said analog signal has a frequency of at least about 2.4 GHz.

35. (Original) A transceiver comprising of the integrated circuit of claim 32.

36. (Original) The transceiver of claim 35 wherein the transceiver is compliant with a standard selected from the group consisting of Institute of Electrical and Electronic Engineers (IEEE) 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11i, 802.11n and 802.16.

37. (Original) A system for broadcasting an analog signal, comprising:
    a) the integrated circuit of Claim 32;
    b) a signal converter configured to provide a converted analog output signal from said output signal of said adjustable amplifier; and
    c) a transmission antenna configured to broadcast said converted analog output signal.

38. (Original) The system of Claim 37, wherein said signal converter comprises a transformer.

39. (Original) The system of Claim 37, further comprising an output capacitor coupled to said second common node.

40. (Original) The system of Claim 37, further comprising an output inductor coupled to said second common node.

41. (Previously Presented) A system for broadcasting an analog signal, comprising:

a) an integrated circuit, comprising:

(1) an adjustable, segmented amplifier, comprising;

(i) a first fixed stage configured to amplify an analog signal and provide a first amplified output at a first common node;

(ii) an adjustable stage comprising a plurality of independently selectable parallel amplifier segments, each of said parallel amplifier segments having an input at said first common node and an output at a second common node, wherein said adjustable stage is configured to provide an output signal in one of a plurality of power ranges corresponding to a number of selected parallel amplifier segments, said output signal having a minimum power efficiency when two or more of said parallel amplifier segments are selected; and

(2) a transmitter communicatively coupled to said adjustable amplifier, said transmitter being configured to transmit said analog signal to said adjustable amplifier;

b) a signal converter configured to provide a converted analog output signal from said output signal of said adjustable amplifier;

c) a transmission antenna configured to broadcast said converted analog output signal;

d) an output inductor coupled to said second common node; and

e) an adjustable resistor coupled to said output inductor.

42. (Original) The system of Claim 37, wherein said output signal comprises a differential signal, and said signal converter is configured to convert said differential signal to a single-ended signal.

43. (Original) The system of Claim 42, further comprising first and second output capacitors, respectively coupled to each line of said differential output signal.

44. (Original) The system of Claim 42, further comprising first and second output inductors, respectively coupled to each line of said differential output signal.

45. (Previously Presented) A system for broadcasting an analog signal, comprising:

a) an integrated circuit, comprising:

(1) an adjustable, segmented amplifier, comprising:

(i) a first fixed stage configured to amplify an analog signal and provide a first amplified output at a first common node;

(ii) an adjustable stage comprising a plurality of independently selectable parallel amplifier segments, each of said parallel amplifier segments having an input at said first common node and an output at a second common node, wherein said adjustable stage is configured to provide an output signal in one of a plurality of power ranges corresponding to a number of selected parallel amplifier segments, said output signal having a minimum power efficiency when two or more of said parallel amplifier segments are selected; and

(2) a transmitter communicatively coupled to said adjustable amplifier, said transmitter being configured to transmit said analog signal to said adjustable amplifier;

b) a signal converter configured to provide a converted analog output signal from said output signal of said adjustable amplifier;

c) a transmission antenna configured to broadcast said converted analog output signal;

d) said signal converter configured to convert said differential signal to a single-ended signal;

e) said output signal comprising a differential signal;

f) first and second output inductors coupled to each line of said output signal; and

g) first and second adjustable resistors respectively coupled to said first and second output inductors.

46. (Original) The system of Claim 44, further comprising a differential output capacitor, respectively coupled to each line of said differential output signal.

47. (Original) A network, comprising:

a) the system of Claim 37; and

b) a receiver in electromagnetic communication with said system.

48. (Original) The network of Claim 47, further comprising a receiving antenna in communication with said receiver.

49. (Original) A network, comprising:

a) a plurality of the systems of Claim 37; and

b) a plurality of receivers, each of said receivers being in communication with at least one of said systems.

50. (Original) The network of Claim 49, wherein at least one of said systems is in communication with at least two of said receivers.

51. (Original) The network of Claim 49, wherein at least two of said systems are in communication with at least one of said receivers.

52. (Original) An integrated circuit, comprising:
    a) the circuit of Claim 18; and
    b) a means for transmitting said analog signal to said adjustable amplifier.

53. (Original) The integrated circuit of Claim 52, wherein said analog signal has a frequency of at least about 2.4 GHz.

54. (Original) A transceiver comprising the integrated circuit of claim 52.

55. (Original) The transceiver of claim 54 wherein the transceiver is compliant with a standard selected from the group consisting of Institute of Electrical and Electronic Engineers (IEEE) 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11i, 802.11n and 802.16.

56. (Original) A system, comprising:
    a) the integrated circuit of Claim 52;
    b) a means for providing said amplified analog output signal from said output signal; and
    c) a means for broadcasting said amplified analog output signal.

57. (Original) The system of Claim 56, wherein said means for providing comprises a pair of inductors in electromagnetic communication with each other.

58. (Original) The system of Claim 56, wherein said output signal comprises a differential signal, and said means for providing is configured to convert said differential signal to a single-ended signal.

59. (Original) A network, comprising:

a) the system of Claim 56; and

b) a means for receiving said amplified analog output signal, in communication with said system.

60. (Original) The network of Claim 59, further comprising a means for processing said amplified analog output signal received by said means for receiving, wherein said means for processing is in communication with said means for receiving.

61. (Original) A network, comprising:

a) a plurality of the systems of Claim 56; and

b) a plurality of means for receiving said amplified analog output signal, each of said means for receiving being in communication with at least one of said systems.

62. (Original) The network of Claim 61, further comprising a plurality of means for processing said amplified analog output signal received by said means for receiving, wherein each of said means for processing is in communication with a unique one of said means for receiving.

63. (Original) The network of Claim 62, wherein at least one of said systems is in communication with at least two of said means for receiving.

64. (Original) The network of Claim 62, wherein at least two of said systems are in communication with at least one of said means for receiving.

65. (Previously Presented) A method of amplifying an analog signal, comprising the steps of:

a) amplifying said analog signal in a fixed amplifier stage;

b) selecting one or more parallel amplifier segments for subsequent signal amplification, wherein each of said parallel amplifier segments comprises (i) a

transistor having a control terminal and (ii) a first inductor configured to resonate with a capacitance at a base of said transistor in electrical communication with said control terminal of said transistor; and

c) amplifying said amplified analog signal with said activated parallel, selectable amplifier segments to generate an output signal in a unique output power range corresponding to the number of selected parallel amplifier segments.

66. (Original) The method of Claim 65, wherein said selecting step comprises applying a bias to the selected amplifier segments.

67. (Previously Presented) The method of Claim 66, further comprising the step of generating said bias.

68. (Previously Presented) The method of Claim 66, further comprising the step of generating said bias independently for each selected parallel amplifier segment.

69. (Previously Presented) The method of Claim 68, wherein a value of said bias corresponds to a number of selected amplifier segments.

70. (Previously Presented) A method of amplifying an analog signal, comprising the steps of:

a) amplifying said analog signal in a fixed amplifier stage;

b) selecting one or more parallel amplifier segments for subsequent signal amplification by applying a bias to the selected amplifier segments, wherein each of said parallel amplifier segments comprises a transistor having a control terminal and a first inductor in electrical communication with said control terminal of said transistor;

c) generating the bias from a programmable current independently for each selected amplifier segment, wherein a value of said bias corresponds to a number of selected amplifier segments;

d) determining a value of said programmable current based on said number of selected amplifier segments; and

e) amplifying said amplified analog signal with said selected amplifier segments to generate an output signal in a unique output power range corresponding to the number of selected amplifier segments.

71. (Currently Amended) A method of amplifying an analog signal, comprising the steps of:

a) amplifying said analog signal in a fixed amplifier stage;

b) selecting one or more independently selectable parallel amplifier segments for subsequent signal amplification, wherein each of said parallel amplifier segments comprises a transistor having a control terminal and a first inductor in electrical communication with said control terminal of said transistor, and selecting one or more of said parallel amplifier segments comprises applying a non-zero bias at said control terminal; and

c) amplifying said amplified analog signal with said selected amplifier segments to generate an output signal in a unique output power range corresponding to the number of selected amplifier segments, wherein said output signal has a minimum power efficiency when two or more of said parallel amplifier segments are selected.

72. (Original) The method of Claim 71, wherein said minimum power efficiency is at least 50% of a maximum efficiency of an amplifier comprising said fixed amplifier stage and said parallel amplifier segments.

73. (Original) The method of Claim 65, further comprising the step of matching a frequency of said output signal to an input of each of said parallel amplifier segments.

74. (Original) The method of Claim 65, further comprising the step of broadcasting said output signal.

75. (Original) The method of Claim 65, wherein said output signal has a minimum frequency of about 800 MHz.

76. (Original) The method of claim 65, wherein the method is compliant with a standard selected from the group consisting of Institute of Electrical and Electronic Engineers (IEEE) 802.11, 802.11a, 802.11b, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

77. (Previously Presented) The adjustable amplifier of Claim 17, wherein said one or more substantially identical characteristics is selected from the group consisting of size, design, layout, gain function, output power, and power efficiency.

78. (Previously Presented) The circuit of Claim 31, wherein said one or more substantially identical characteristics is selected from the group consisting of size, design, layout, gain function, output power, and power efficiency.

79. (Previously Presented) The adjustable amplifier of Claim 1, wherein said adjustable stage is further configured for class AB operation.

80. (Canceled)

81. (New) The adjustable amplifier of Claim 9, wherein said input of said parallel amplifier segments is in phase at said first common node.

82. (New) The adjustable amplifier of Claim 9, wherein said outputs of said parallel amplifier segments are summed at said second common node.

83. (New) The adjustable amplifier of Claim 9, configured for class AB operation.

84. (New) The adjustable amplifier of Claim 9, wherein each of said transistors comprises a bipolar junction transistor.

85. (New) The adjustable amplifier of Claim 9, wherein said amplifier receives a direct current bias signal as said analog signal.

86. (New) The method of Claim 71, wherein said selected amplifier segments amplifying said amplified analog signal in phase.

87. (New) The method of Claim 71, further comprising summing outputs of said selected amplifier segments to form said output signal.

88. (New) The method of Claim 71, wherein said a combination of said fixed amplifier stage and one or more parallel amplifier segments is configured for class AB operation.

89. (New) The method of Claim 71, wherein said transistor comprises a bipolar junction transistor.

90. (New) The method of Claim 71, wherein said amplifier receives a direct current bias signal as said analog signal.